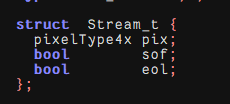
Advanced SoC Lab2-2

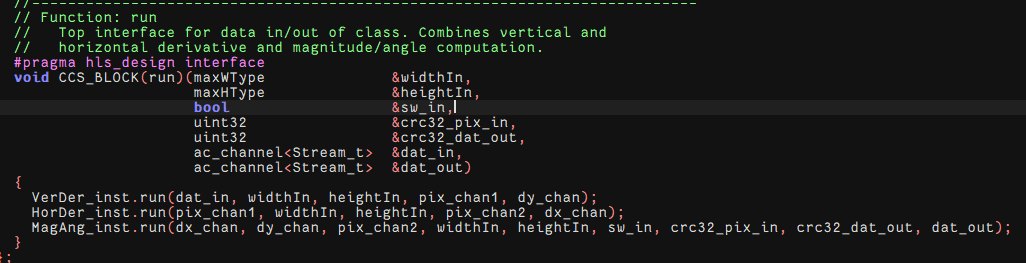
組別:第四組

1. How you design your work ( 5 modifications) .
   1. **Process four pixels per clock cycle.**

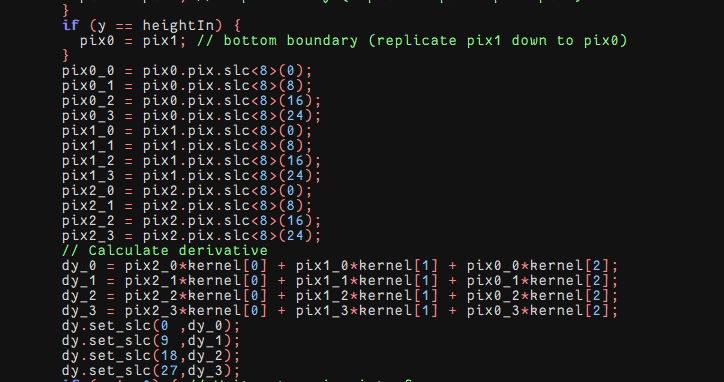
首先，定義一個具有4 pixels、eol、sof 的Data type



Top module 的Data in 修改成該Data type (Stream\_t)



將原本1 pixel 的運算擴展 4倍。

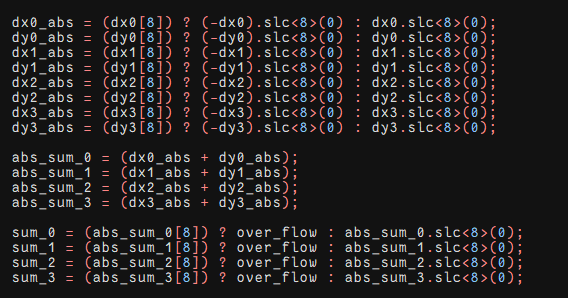


* 1. **Use sum of absolute difference (SAD) for edge magnitude calculation.**

透過sign bit 去判斷該數的正負。

如果sign bit = 0，維持不變。

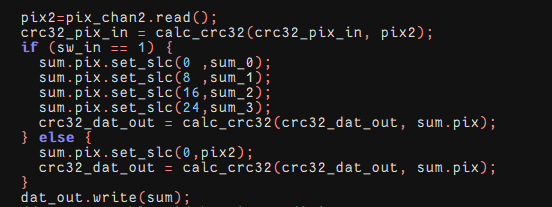
如果sign bit = 1，則取負數，使其該數變為正數。



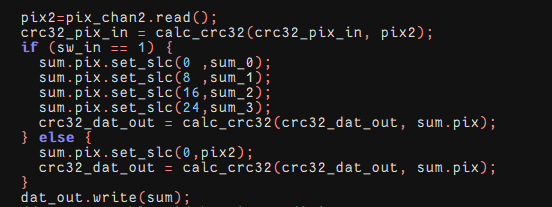
* 1. **Add two crc32 calculation on image input / output.**

設置初始值為 0xFFFFFFFF

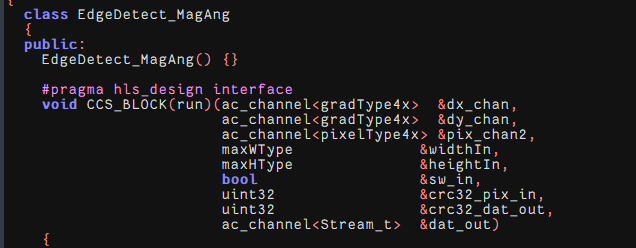


接著，再將輸出結果(sum) 透過calc\_crc32 進行運算。

* 1. **Select the output source from input image or the calculated magnitude.**

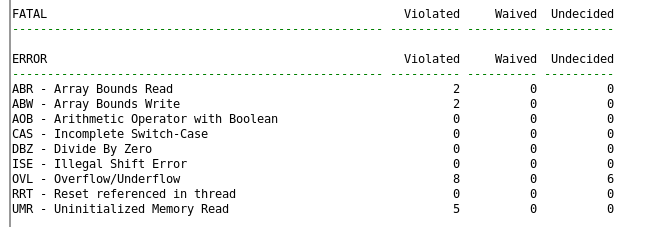
透過sw\_in判斷輸出結果(sum)應該為 Edge\_map (sum\_0,sum\_1, sum\_2, sum\_3) 還是 Orig. Img (pix2)。

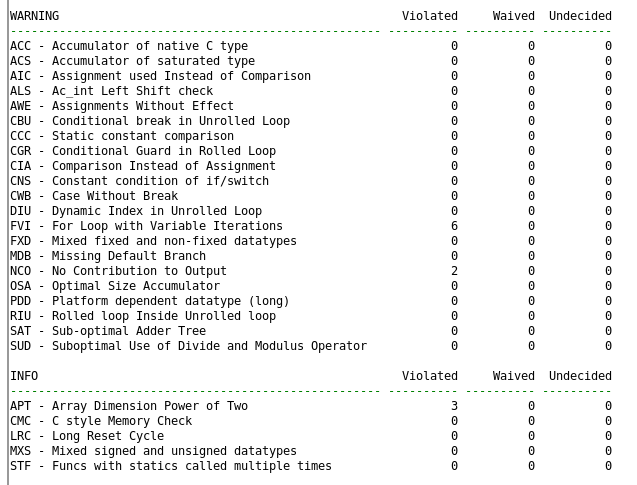
* 1. **Remove the angle calculation.**

將angle output 刪除

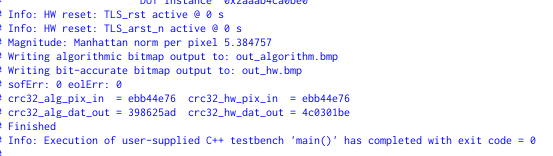
1. What’s the test result of catapult design(C design checker, testbench)

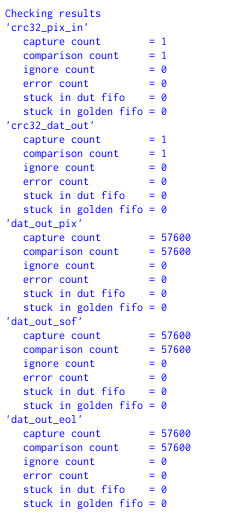
C design checker:





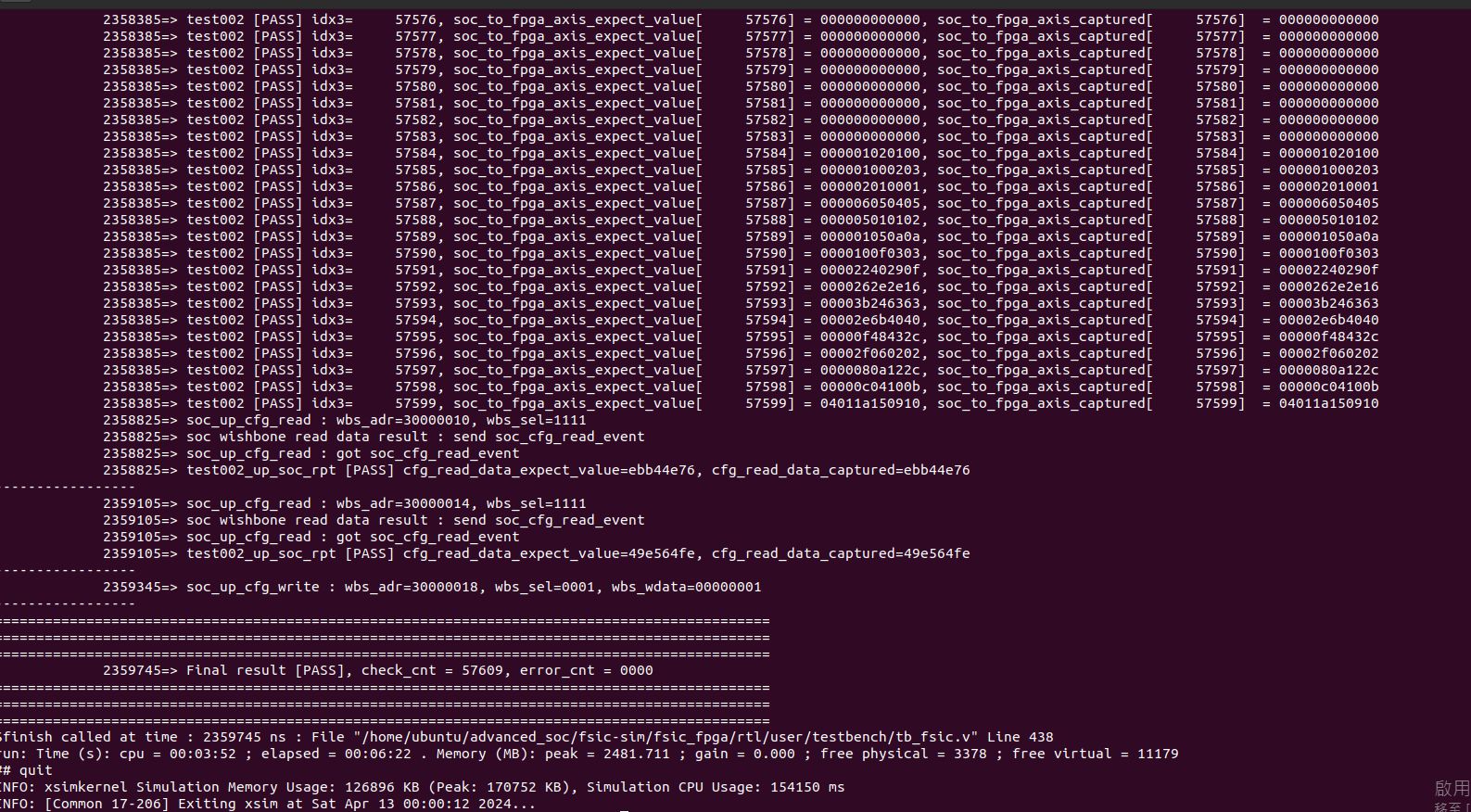
Testbench:





1. How to integrate your design in FSIC
2. What’s the simulation result of FSIC

SW\_IN = 1 (Edge Map)



SW\_IN = 0 (Orig. Img)

